DATA SHEET

P83CL887; P87CL887
TELX microcontrollers for CT0 handset/basestation applications

Preliminary specification
File under Integrated Circuits, IC20

1997 Oct 30

Philips Semiconductors

PHILIPS

CONTENTS

1 FEATURES
2 GENERAL DESCRIPTION
3 ORDERING INFORMATION
4 BLOCK DIAGRAM
5 PINNING INFORMATION
5.1 Pinning
5.2 Pin description
6 FUNCTIONAL DESCRIPTION
6.1 Special Function Registers (SFRs)
6.2 I/O facilities
6.2.1 Ports
6.2.2 Port I/O configuration
6.2.3 Alternative Port Function Register (ALTP)
6.3 Timer/event counters
6.3.1 Timer T2
6.3.2 Timer/Counter 2 Control Register (T2CON)
6.4 MSK modem
6.5 Watchdog Timer (T3)
6.6 OTP programming
6.6.1 OTP programming by a programmer
6.6.2 In System Programming mode
6.7 Oscillator circuitry
6.7.1 Resonator requirements
6.7.2 Recommended resonator types
6.8 Emulation
6.9 Read-Modify-Write bug
6.9.1 Example 1 writing ‘directly’ to a port
6.9.2 Example 2: Setting one bit of the port
7 LIMITING VALUES
8 CHARACTERISTICS
9 PACKAGE OUTLINE
10 SOLDERING
10.1 Introduction
10.2 Reflow soldering
10.3 Wave soldering
10.4 Repairing soldered joints
11 DEFINITIONS
12 LIFE SUPPORT APPLICATIONS
13 PURCHASE OF PHILIPS I^{2}C COMPONENTS

1 FEATURES

- Full static 80C51 CPU; enhanced 8-bit architecture with:
  - Minimum 6 cycles per instruction (twice as fast as a standard 80C51 core)
  - Non-page oriented instructions
  - Direct addressing
  - Four 8-byte RAM register banks
  - Stack depth limited only by available internal RAM (maximum 256 bytes)
  - Multiply, divide, subtract and compare instructions
- Three 8-bit ports (18 I/O lines)
- Program Memory:
  - P87CL887: 12 kbytes One Time Programmable
  - P83CL887: 12 kbytes ROM
- 512 bytes RAM
- Amplitude Controlled Oscillator (ACO) suitable for quartz crystal or ceramic resonator
- Improved Power-on/Power-off reset (POR) circuitry
- Low Voltage Detection (LVD) with 11 software programmable levels
- Eight interrupts on Port 1:
  - Edge or level sensitive triggering selectable via software
  - Power-saving use for keyboard control
- Twenty source, twenty vector interrupt structure with two priority levels
- Wake-up from Power-down mode via LVD or external interrupts at Port 1
- DTMF generator
- MSK modem including Manchester encoder/decoder with 2 digital outputs for analog cordless telephones (standards CT0/CT1/CT1+)
- Watchdog Timer
- Two standard 16-bit timer/event counters
- Additional 16-bit timer/event counter with Capture, Compare and Auto-reload function
- Full duplex enhanced UART with double buffering
- I^2C-bus interface for serial transfer on two lines, maximum 400 kHz
- Very low current consumption
- Single supply voltage: 2.7 to 3.6 V
- Frequency: 3.58 MHz
- Operating temperature: –25 to +70 °C
- 28 pin SO package.

2 GENERAL DESCRIPTION

The P8xCL887 (denoting the P83CL887 and P87CL887) are manufactured in an advanced CMOS technology and are 8-bit microcontrollers especially suited for low cost analog cordless telephone applications (CT0, CT1 and CT1+ standards). Consequently, features like DTMF, MSK modem and POR/LVD are integrated on-chip.

Both devices are optimized for low power consumption and in addition have two software selectable modes for further power reduction: Idle and Power-down modes. All derivative blocks can switch off their clock if they are inactive.

The instruction set of the P8xCL887 is based on that of the 80C51. The P8xCL887 also function as arithmetic processors having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. As port P2 is not implemented there is no external data or memory access and MOVX operations cannot be used.

This data sheet details the specific properties of the P8xCL887; for details of the P8xCL887 core and the derivative functions see the *“TELX family”* data sheet and *“Data Handbook IC20”*.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P83CL887DFT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
P87CL887DFT			

4 BLOCK DIAGRAM

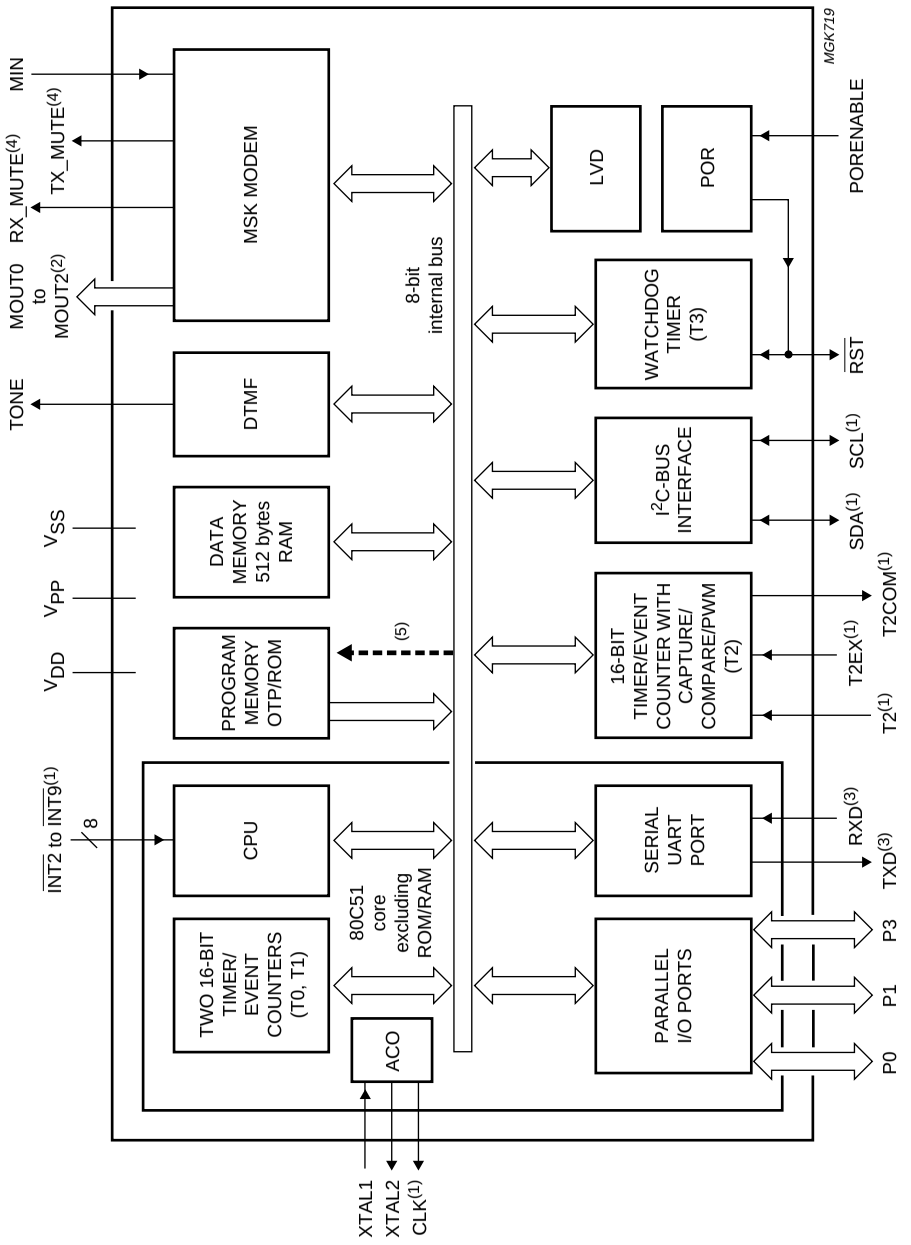


Fig.1 Block diagram.

(1) Alternative functions of Port 1.
(2) MOUT0 is the alternative function to P3.1.
(3) Alternative function of Port 3.
(4) By software any I/O port pin can be used.
(5) In-circuit OTP programming.

5 PINNING INFORMATION

5.1 Pinning

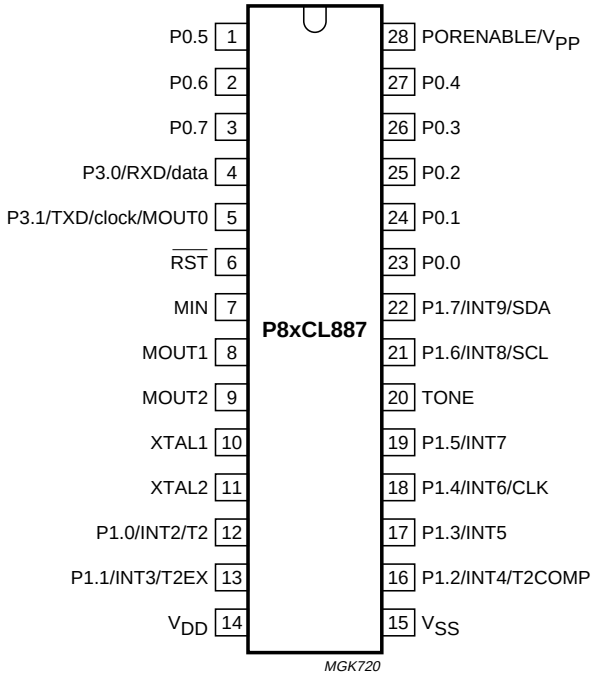


Fig.2 Pin configuration.

5.2 Pin description

Table 1 SO28 package

SYMBOL	PIN	DESCRIPTION
$\overline{RST}$	6	**Active low reset:** a LOW level on this pin for two machine cycles while the oscillator is running, resets the device. The $\overline{RST}$ pin is also an output which can be used to reset other ICs.
MIN	7	Digital **MSK** modem input.
MOUT1	8	Digital **MSK** modem outputs.
MOUT2	9	
XTAL1	10	**Crystal input:** Input to the Amplitude Controlled Oscillator. Also the input for an externally generated clock source.
XTAL2	11	**Crystal output:** Output of the Amplitude Controlled Oscillator; to be left non-connected when an external oscillator clock is used.
V_{DD}	14	Power supply.
V_{SS}	15	Ground.
P0.0 to P0.7	23 to 27, 1 to 3	**Port 0:** 8-bit bidirectional I/O port; every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2.
P1.0/INT2/T2	12	**Port 1:** 8-bit bidirectional I/O port with alternative functions. Every port pin except P1.6 and P1.7 (I^2C-bus pins) can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. Port P1.3 has LED drive capability. Port 1 also serves the alternative functions: **INT2 to INT9** interrupts; Timer T2 external inputs **T2** and **T2EX**; Timer T2 compare output **T2COMP**; external clock output **CLK**; I^2C-bus clock **SCL** and data in/outputs **SDA**.
P1.1/INT3/T2EX	13	
P1.2/INT4/T2COMP	16	
P1.3/INT5	17	
P1.4/INT6/CLK	18	
P1.5/INT7	19	
P1.6/INT8/SCL	21	
P1.7/INT9/SDA	22	
P3.0/RXD/data	4	**Port 3:** 3 or 2-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Chapter 6.2. Port 3 also serves the alternative functions: **RXD/data** is the serial port receiver data input (asynchronous) or data I/O (synchronous); **TXD/clock** is the serial port transmitter data output (asynchronous) or clock output (synchronous) or digital MSK modem output **MOUT0**.
P3.1/TXD/clock/ MOUT0	5	
TONE	20	**DTMF** output.
PORENABLE/V_{PP}	28	**PORENABLE**: Power-on-reset circuit enable. If PORENABLE = 1, the internal Power-on-reset circuit is enabled. If external reset circuitry is used, it is recommended to keep PORENABLE = 0 to reach lowest power consumption. This pin is also used for the OTP programming voltage V_{PP}.

6 FUNCTIONAL DESCRIPTION

6.1 Special Function Registers

Table 2 Special Function Registers memory map and reset values

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE(1)
80C51 core			
Accumulator	ACC	E0H	0000 0000
B Register	B	F0H	0000 0000
Data Pointer Low byte	DPL	82H	0000 0000
Data Pointer High byte	DPH	83H	0000 0000
Program Counter High byte	PCH	no SFR	0000 0000
Program Counter Low byte	PCL	no SFR	0000 0000
Power Control Register	PCON	87H	0000 0000
Prescaler Register	PRESC	F3H	0000 0000
Program Status Word	PSW	D0H	0000 0000
Stack Pointer	SP	81H	0000 0111
Timer 0 and Timer 1			
Timer/Counter Control Register	TCON	88H	0000 0000
Timer/Counter 0 High byte	TH0	8CH	0000 0000
Timer/Counter 1 High byte	TH1	8DH	0000 0000
Timer/Counter 0 Low byte	TL0	8AH	0000 0000
Timer/Counter 1 Low byte	TL1	8BH	0000 0000
Timer/Counter Mode Control Register	TMOD	89H	0000 0000
Ports			
Alternative Port Function Control Register	ALTP	A3H	0000 0000
Port P0 Output Data Register	P0	80H	1111 1111
Port P0 Configuration A Register	P0CFGA	8EH	1111 1111
Port P0 Configuration B Register	P0CFGB	8FH	0000 0000
Port P1 Output Data Register	P1	90H	1111 1111
Port P1 Configuration A Register	P1CFGA	9EH	0011 1111
Port P1 Configuration B Register	P1CFGB	9FH	0000 0000
Port P3 Output Data Register	P3	B0H	XXXX XX11
Port P3 Configuration A Register	P3CFGA	BEH	XXXX XX11
Port P3 Configuration B Register	P3CFGB	BFH	XXXX XX00
Port P4 Output Data Register	P4	C1H	XXXX XXX0(2)

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE(1)
Timer 2			
Timer 2 Compare High byte	COMP2H	ABH	0000 0000
Timer 2 Compare Low byte	COMP2L	AAH	0000 0000
Timer 2 Reload/Capture High byte	RCAP2H	CBH	0000 0000
Timer 2 Reload/Capture Low byte	RCAP2L	CAH	0000 0000
Timer/Counter 2 Control Register	T2CON	C8H	0000 0000
Timer/Counter 2 High byte	TH2	CDH	0000 0000
Timer/Counter 2 Low byte	TL2	CCH	0000 0000
DTMF			
High Group Frequency Register	HGF	A2H	0000 0000
Low Group Frequency Register	LGF	A1H	0000 0000
Interrupt logic			
Interrupt Enable Register 0	IEN0	A8H	0000 0000
Interrupt Enable Register 1	IEN1	E8H	0000 0000
Interrupt Enable Register 2	IEN2	F1H	0000 0000
Interrupt Priority Register 0	IP0	B8H	0000 0000
Interrupt Priority Register 1	IP1	F8H	0000 0000
Interrupt Priority Register 2	IP2	F9H	0000 0000
Interrupt Sensitivity Register 1	ISE1	E1H	0000 0000
Interrupt Polarity Register	IX1	E9H	0000 0000
Interrupt Request Flag Register 1	IRQ1	C0H	0000 0000
Low Voltage Detection			
LVD Control Register	LVDCON	F2H	0000 0000
POR/ACO			
Reset Status Register	RSTAT	E6H	XXX0 1001(3)
MSK modem			
MSK Modem Control Register	MCON	D3H	0000 0000
MSK Modem Data Buffer	MBUF	D1H	XXXX XXXX
MSK Modem Status Register	MSTAT	D2H	XX00 0000

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE(1)
UART			
Serial Port Buffer	S0BUF	99H	0000 0000
Serial Port Control Register	S0CON	98H	0000 0000
I^2C-bus interface			
Address Register	S1ADR	DBH	0000 0000
Serial Control Register	S1CON	D8H	0000 0000
Data Shift Register	S1DAT	DAH	0000 0000
Serial Status Register	S1STA	D9H	1111 1000
Watchdog Timer			
Watchdog Timer Control Register	WDCON	A5H	1010 0101
Watchdog Timer Interval Register	WDTIM	FFH	0000 0000
OTP interface			
OTP Address High Register	OAH	D5H	X00X XXXX
OTP Address Low Register	OAL	D4H	XXXX XXXX
OTP Data Register	ODATA	D6H	XXXX XXXX
OTP In System Programming Register	OISYS	DCH	000X 0000
OTP Test Register	OTEST	C7H	0000 0000
Reserved locations, see note 4			
–	–	E7H, FDH	–

Notes

1. Where: X = undefined state or not implemented bit.
2. Only used to define MSK input polarity. Write only.
3. Defined by mask.
4. E7H and FDH are reserved locations and must not be written to.

6.2 I/O facilities

6.2.1 PORTS

The P8xCL887 have 18 I/O lines, treated as 18 individually addressable bits or as three parallel 8-bit addressable ports. The alternative functions are detailed below:

Port 0 Offers no alternative functions.

Port 1 Used for a number of special functions:

- P1.0 to P1.7 provides the inputs for the external interrupts INT2 to INT9
- P1.2/T2COMP for external activation and Compare/Auto-reload output function of Timer 2
- P1.4/CLK for the clock output
- P1.6/SCL and P1.7/SDA for the I^2C-bus interface are real open-drain outputs or high-impedance; no other port configurations are available.

Port 2 Not available.

Port 3 Pins can be configured individually to provide:

- P3.0/RXD/data and P3.1/TXD/clock/MOUT0 are serial port receiver input and transmitter output (UART).

To enable a Port pin alternative function, the Port bit latch in its SFR must contain a logic 1.

Each port consists of a latch (Special Function Registers P0 to P3), an output driver and input buffer. All ports have internal pull-ups. Figure 3b shows that the strong transistor ‘p1’ is turned on for only one oscillator period after a LOW-to-HIGH transition in the port latch. When on, it turns on ‘p3’ (a weak pull-up) through the inverter IN1. This inverter and transistor ‘p3’ form a latch which holds the logic 1.

Port P1.3 has LED drive capability.

6.2.2 PORT I/O CONFIGURATION

I/O port output configurations are determined by the settings in the port configuration SFRs. There are 2 SFRs for each port: PnCFGA and PnCFGB, where ‘n’ indicates the specific port number (0 to 3).

One bit in each of the 2 SFRs relates to the output setting for the corresponding port pin, allowing any combination of the 2 output types to be mixed on those port pins. For instance, the output type of Port 1 pin 3 is controlled by the setting of bit 3 in the SFRs P1CFGA and P1CFGB.

The port pins may be individually configured via SFRs with one of the following modes (P1.6 and P1.7 can be open-drain or high-impedance but never have any diodes against V_{DD}). These modes are also shown in Fig.3.

Mode 0 Open-drain; quasi-bidirectional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor; e.g. Port 0 for external memory accesses (EA = 0) or access above the built-in memory boundary. The ESD protection diodes against V_{DD} and V_{SS} are still present; see Fig.3b Except for the I^2C pins P1.6 and P1.7, ports which are configured as open-drain still have a protection diode to V_{DD}.

Mode 1 Standard port; quasi-bidirectional I/O with pull-up. The strong pull-up ‘p1’ is turned on for only two oscillator periods after a LOW-to-HIGH transition in the port latch. After these two oscillator periods the port is only weakly driven through ‘p2’ and ‘very weakly’ driven through ‘p3’ see Fig.3b.

Mode 2 High-impedance; this mode turns off all output drivers on a port. Thus, the pin will not source or sink current and may be used as an input-only pin with no internal drivers for an external device to overcome see Fig.3c.

Mode 3 Push-pull; output with drive capability in both polarities. Under this mode, pins can only be used as outputs see Fig.3d.

Tables 3 and 4 show the configuration register settings for the 4 port output types.

The electrical characteristics of each output type can be found in Chapter 8. The default port configuration after reset is given in Table 4.

Table 3 Port Configuration Registers PnCFGA and PnCFGB (n = 0, 1 and 3) settings

MODE(1)	PnCFGA	PnCFGB	PORT OUTPUT CONFIGURATION	
			NORMAL PORTS	I²C-BUS PORTS (P1.6 AND P1.7)
Mode 0	0	0	open-drain	open-drain
Mode 1	1	0	quasi-bidirectional	open-drain
Mode 2	0	1	high-impedance	high-impedance
Mode 3	1	1	push-pull	open-drain

Note

1. Mode changes may cause glitches to occur during transitions. When modifying both registers, WRITE instructions should be carried out consecutively.

Table 4 Special Function Registers for port configurations/data

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS (HEX)	STATE AFTER RESET
Port P0 Output Data(1)	P0	80	1111 1111
Port P0 Configuration A	P0CFGA	8E	1111 1111
Port P0 Configuration B	P0CFGB	8F	0000 0000
Port P1 Output Data(1)	P1	90	1111 1111
Port P1 Configuration A	P1CFGA	9E	0011 1111
Port P1 Configuration B	P1CFGB	9F	0000 0000
Port P3 Output Data(1)	P3	B0	XXXX XX11
Port P3 Configuration A	P3CFGA	BE	XXXX XX11
Port P3 Configuration B	P3CFGB	BF	XXXX XX00

Note

1. This means that P0, P1.0 to P1.5 and P3 are initialized in Mode 1 (quasi-bidirectional, driving a weak HIGH) and the I²C-bus ports P1.6 and P1.7 are initialized in Mode 0 (open-drain, not driven).

6.2.3 Alternative Port Function Control Register (ALTP)

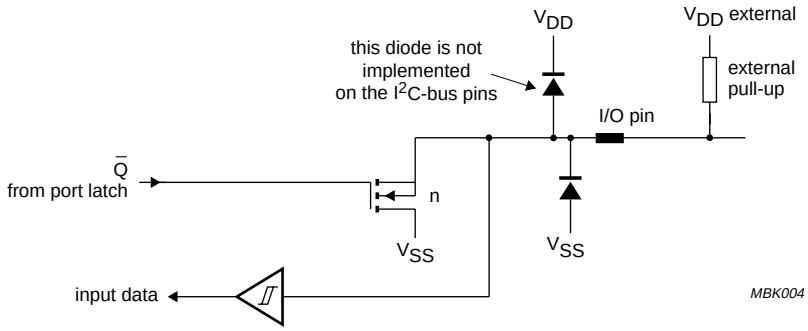
This 4-bit register controls the alternative functions of certain port pins.

Table 5 Alternative Port Function Register (SFR address A3H)

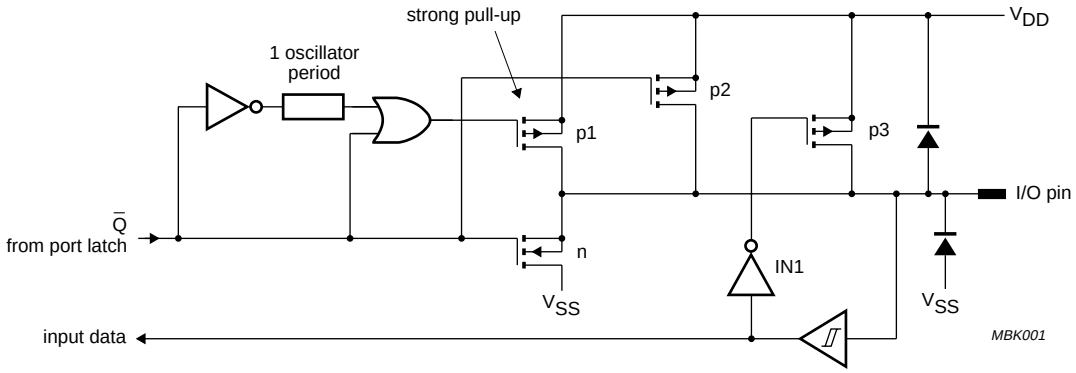
7	6	5	4	3	2	1	0
–	–	–	–	EMOUT0	ECLK	EMLDY	ETONE

Table 6 Description of ALTP bits

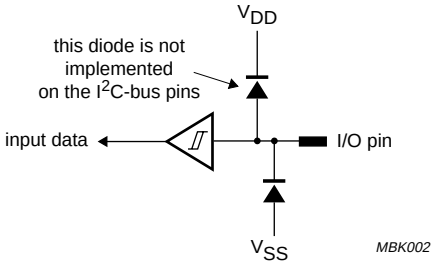
BIT	SYMBOL	DESCRIPTION
7 to 4	–	Reserved.
3	EMOUT0	**Enable MOUT0.** If this bit is set, P3.1 will output the MOUT0 signal.
2	ECLK	**Enable Clock.** If this bit is set, P1.4 is configured to be push-pull, and P1.4 will output the system clock.
1	EMLDY	**Enable MLDY.** If this bit is set, P1.5 is configured to be push-pull, and P1.5 will output the digital MLDY signal of the DTMF generator.
0	ETONE	**Enable TONE.** If this bit is set, the TONE output of the DTMF generator is enabled.



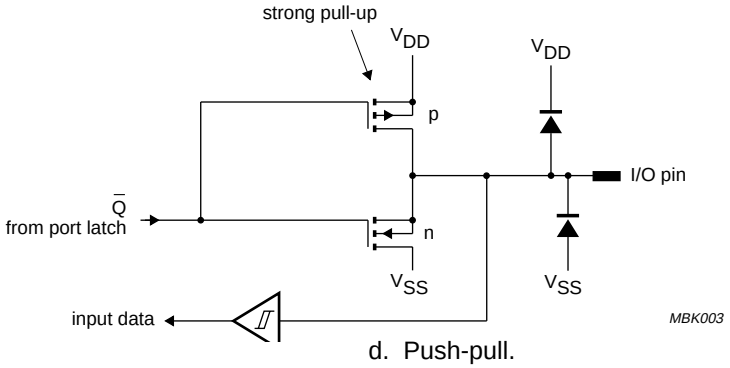
a. Open-drain.



b. Standard/quasi-bidirectional.



c. High-impedance.



d. Push-pull.

Fig.3 Port configuration options.

6.3 Timer/event counters

The P8xCL887 contain three 16-bit timer/event counters: Timer 0, Timer 1 and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events (T2 only, no external input for T0/T1)
- Generate interrupt requests
- Generate output on comparator match.

In the 'timer' mode the register is incremented every machine cycle.

Since a machine cycle consists of minimum 6 oscillator periods, the maximum count rate is $\frac{1}{6} \times f_{osc}$.

In the 'counter' mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes one machine cycle (minimum 6 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $\frac{1}{6} \times f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time-interval or event counter.

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.

Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

6.3.1 TIMER T2

Note that the timer T2 of the P8xCL887 deviates from the timer T2 described in the *"TELX family"* data sheet.

Timer T2 is a 16-bit timer/counter that can operate either as a timer or as an event counter. These functions are selected by the state of the C/$\overline{T2}$ bit in the T2CON register. Five operating modes are available:

- Capture
- Compare
- Auto-reload
- Compare with Auto-reload
- Capture and Compare.

These modes are selected via the T2CON register.

6.3.1.1 Capture mode

In the Capture mode, two options may be selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2, this may then be used to generate an interrupt.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX causes the current value in TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes the EXF2 bit in T2CON to be set; this may also be used to generate an interrupt.

The Capture mode is shown in Fig.4.

6.3.1.2 Compare mode

In the Compare mode, each time timer T2 is incremented, the contents of the compare registers COMP2H and COMP2L are compared with the new counter value of timer T2. When a match occurs, the interrupt flag COMP in register T2CON and port bit P1.2 are toggled. The 16-bit value held in these registers is preset by software. The first toggle after a reset will set the flag COMP. The Compare mode is shown in Fig.4.

6.3.1.3 Auto-reload mode

In the Auto-reload mode there are also two options selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then when Timer 2 rolls over, it sets the TF2 bit but also causes the Timer 2 registers to be reloaded with the 16-bit value held in registers RCAP2L and RCAP2H. The 16-bit value held in these registers is preset by software.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX will also trigger the 16-bit reload and set the EXF2 bit.

6.3.1.4 Compare with Auto-reload mode

The Auto-reload mode can be used together with the Compare mode. The Auto-reload modes are shown in Fig.5.

6.3.1.5 Capture and Compare modes

The Capture and the Compare mode of timer T2 can be used separately or simultaneously. The function is chosen via the bits ECOMP, CP/$\overline{RL2}$ and TR2 in register T2CON.

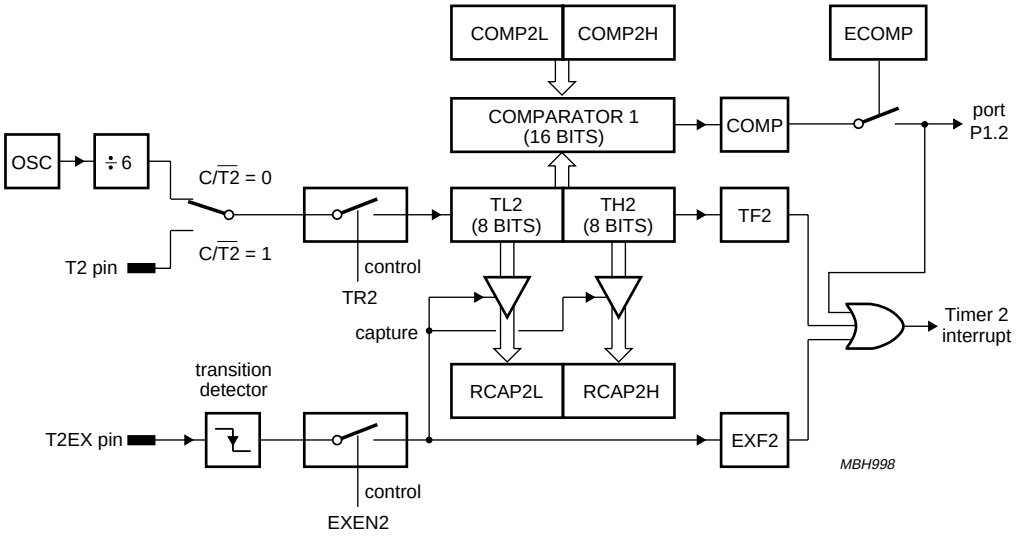


Fig.4 Timer 2 in Capture and/or Compare mode.

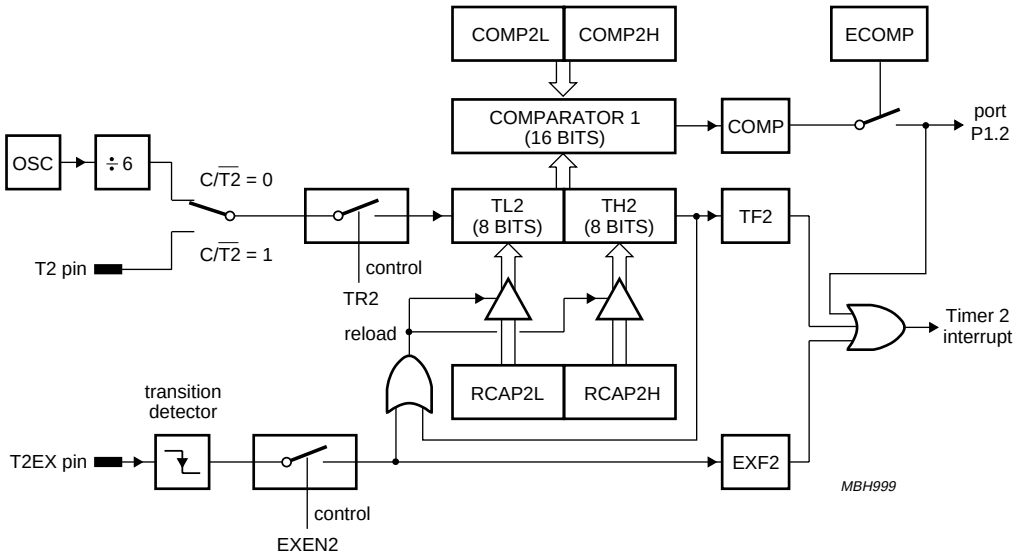


Fig.5 Timer 2 in Auto-Reload with/without Compare mode.

6.3.2 Timer/Counter 2 Control Register (T2CON)

Table 7 Timer/Counter 2 Control Register (SFR address C8H)

7	6	5	4	3	2	1	0
TF2	EXF2	COMP	ECOMP	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 8 Description of T2CON bits

BIT	SYMBOL	DESCRIPTION
7	TF2	**Timer 2 overflow flag.** TF2 is set by a Timer 2 overflow and must be cleared by software.
6	EXF2	**Timer 2 external flag.** EXF2 is set when either a capture or reload is caused by a negative transition on T2EX and when EXEN2 = 1. When Timer T2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. EXF2 must be cleared by software.
5	COMP	**Interrupt flag**. When a match between the 16-bit compare register (COMP2L and COMP2H) and the new counter value of timer T2 occurs, the interrupt flag COMP in register T2CON and port bit P1.2 are toggled.
4	ECOMP	**Enable compare output bit.** When set by software, the controller toggles port bit P1.2 (T2COMP) when a compare match occurs.
3	EXEN2	**Timer 2 external enable flag.** When set, allows a capture or reload to occur as a result of a negative transition on T2EX. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	TR2	**Timer 2 start/stop control.** Control bit for Timer 2.
1	C/$\overline{T2}$	**Timer 2 timer or counter select.** C/$\overline{T2}$ = 0 selects the internal timer with a clock frequency of $\frac{1}{6} \times f_{osc}$. C/$\overline{T2}$ = 1 selects the external event counter; negative edge-triggered.
0	CP/$\overline{RL2}$	**Capture/reload flag.** When set captures will occur on negative transitions at T2EX, if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1.

Table 9 Timer 2 operating modes

ECOMP	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	0	1	16-bit Compare
1	1	1	16-bit Capture and Compare
1	0	0	16-bit Compare with Auto-reload
0	0	0	off

6.4 MSK modem

For the P8xCL887, MIN has its own dedicated pin and is no longer the alternative function of P4.0. The polarity of MIN can however still be programmed with the P4.0 bit. P4.0 is a data SFR but no port logic is connected.

Only the most significant bits of MOUT, i.e. MOUT2 and MOUT1 are directly available as separate pins. In order to be able to further increase the signal quality, the MOUT0 signal is available as alternative port function of P3.1.

For controlling this alternative port function the EMOUT0 bit has been added to the Alternative Port Function Register (ALTP); see Section 6.2.3.

6.5 Watchdog Timer (T3)

The Watchdog Timer differs from the description given in the *"TELX family"* data sheet in that the external $\overline{EW}$ pin does not exist on the P8xCL887.

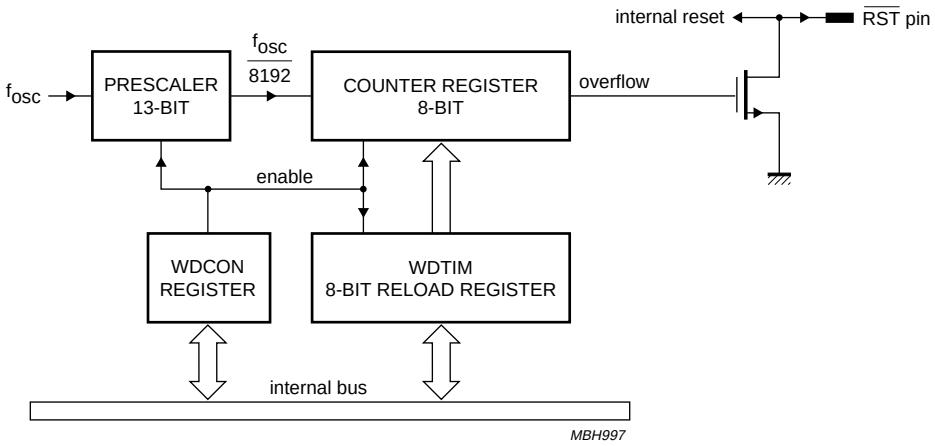


Fig.6 Functional diagram of the Watchdog Timer.

6.6 OTP programming

6.6.1 OTP PROGRAMMING BY A PROGRAMMER

The 12 kbytes One Time Programmable (OTP) memory can be programmed by using a programmer (OM4260) together with a programmer adapter OM5508. Since the memory is programmable only once, programming an already programmed address results in a logical AND of the old and new code. The OTP code can be read out by the programmer for verification.

6.6.1.1 Signature bytes

The OTP memory contains three signature bytes which can be read by the programmer to identify the device. A special address space has been used for these bytes which does not influence the user address space.

The values of the signature bytes are:

(030H) = 15H, indicates manufactured by Philips Semiconductors

(031H) = C8H, indicates P87CL887

(060H) = 00H, currently not used.

6.6.1.2 Security

The following protection levels are available to protect TELX applications against software piracy and unwanted access to data stored in the application.

1. Preventing programming of an already programmed OTP. Note that security Level 1 also disables In System Programming.
2. Preventing the reading of program code in OTP by disabling access of the programmer to the Program Memory. Also verification of code during In System Programming is disabled. In this mode signature and security level verification is still possible.
3. This level has the same functionality as Level 2.

Table 10 describes how these protection levels can be selected by programming the three least significant bits of the security byte.

Table 10 Protection level selection

BITS	LEVEL	DESCRIPTION
UUU	0	no security
UUP	1	Level 1 is activated
UPP	2	Levels 1 and 2 are activated
PPP	3	Levels 1, 2 and 3 are activated

6.6.2 IN SYSTEM PROGRAMMING MODE

In the In System Programming mode the OTP can be programmed under the control of the CPU. A control program must be available in the OTP. This mode can be used to program several bytes in the OTP if the chip is already in a system e.g. to store tuning parameters.

In the In System Programming mode the complete address space OTP can be programmed.

The user should take care not to overwrite the existing code.

For In System Programming four SFRs are used to control the OTP.

Table 11 SFRs for In System Programming

SFR NAME	DESCRIPTION
OAH	OTP Address High Register
OAL	OTP Address Low Register
ODATA	OTP Data Register
OISYS	OTP In System Register; see Section 6.6.2.5

6.6.2.1 Mode entry

The In System Programming mode is entered by setting the InSysMode bit of the OISYS SFR. The I^2C-bus is used for data transfer in this mode. If the I^2C-bus interface is addressed by an external master, the interface generates an interrupt request. The interrupt handler can now read the OISYS SFR and determine the status of the external high voltage (VPon). If high voltage is not present the interrupt is a standard I^2C-bus interrupt.

If high voltage is present the In System Program interrupt routine has to start writing the InSysMode bit (OISYS.0) and controls the address and data transfer.

During In System Programming the OTP memory has to be in DC read mode. This is achieved by writing 08H to the OTEST SFR. If the In System Programming mode is left, 00H must be written into the OTEST SFR.

The program voltage has to be available and stable for at least 10 µs before the mode is entered and must remain stable until the circuit has left the In System Programming mode. The high voltage can be applied for maximum 60 seconds during the complete lifetime of the circuit.

6.6.2.2 Program cycle

The data and address have to be supplied to the microcontroller and the control program must write to the SFRs: ODATA, OAH and OAL. A timer has to be initialized for a 100 μs cycle and the WE bit of the OISYS SFR has to be set. Now the core must be set into the Idle mode. As long as the circuit is in Idle mode a programming pulse is applied. After the interrupt request of the timer the OTP is available for normal code fetching.

The address applied to the OAH and OAL SFRs must be in the 12 kbytes address space.

6.6.2.3 Verify for In System Programming

Verify is done in a similar way as programming. The circuit is put into the Idle mode and at the start of this mode the sense amplifiers are switched to verify mode and a read cycle is started. The timer has to be initialized for a cycle of at least 1 μs. The address is supplied by the SFRs OAH and OAL. The WE bit of the OISYS SFR has to be reset. The OTP output data is latched in the ODATA SFR. After Idle mode is finished this SFR can be read in the normal way.

To be sure that the verified data is written into the SFR it is advised to write FFH into the ODATA SFR before a verify is started.

6.6.2.4 Signature bytes and security

Signature bytes can be read by setting the SIG bit of the OISYS SFR and applying the address of the signature byte. Applying a write pulse while the SIG bit of the OISYS SFR is HIGH is forbidden although the contents of the signature bytes will never be destroyed. The signature bytes (and other test addresses) are always readable independent of the security.

Security has the same meaning as in Parallel Program mode. Security can be programmed and verified by setting the SEC bit of the OISYS SFR. The security bits can be programmed like normal bits. To program Level 1, 01H must be loaded in the ODATA SFR. These values are 03H and 07H for Level 2 and Level 3 respectively. The SEC bit of the OISYS SFR must be HIGH during the program cycle. Loading an address is not necessary. The timer must be initialized for 200 μs instead of 100 μs for security or two standard pulses must be applied. If the SEC bit is HIGH during verify, the security bits can be read from the ODATA SFR. Verifying a normal address while security level (Level 2 or Level 3) has been programmed will result in reading 00H.

Verifying is disabled immediately after programming Level 2 or Level 3. Programming is disabled if a verify or a reset is applied after programming security level: Level 1 or higher.

6.6.2.5 OTP In System Programming Register (OISYS)

The OISYS SFR controls the In System Programming mode. The data to be programmed is stored in the SFR ODATA and the address for this data in the SFRs OAH and OAL.

Table 12 OTP In System Programming Register (SFR address DCH)

7	6	5	4	3	2	1	0
–	–	–	VPon	SEC	SIG	WE	InSysMode

Table 13 Description of OISYS bits

BIT	SYMBOL	DESCRIPTION
7 to 5	–	reserved
4	VPon	V_{PP} status (read only)
3	SEC	security bits enable
2	SIG	signature bytes enable
1	WE	Write Enable, enables programming
0	InSysMode	In System Programming status bit

6.6.2.6 How to connect the PORENABLE/V_{PP} pin in the In System Programming mode

If the V_{PP} pin is dual-mode (e.g. PORENABLE/V_{PP}), ICs connected to the signal PORENABLE **must be able to withstand up to 13 V**, i.e. cannot have clamping diodes or low break-down voltages. If the pin is connected to a fixed voltage (V_{DD} or V_{SS}) there must be a way of switching-off this connection on the PCB. A possible implementation is presented in Fig.7.

In the example (see Fig.7) the POR is enabled in normal mode of operation (pin PORENABLE/V_{PP} = 1 by the pull-up), but the V_{PP} source must supply enough current in R_p in order to guarantee a minimum of 12.5 V on the PORENABLE/V_{PP} pin.

Note that if in the application the Power-on-reset is disabled (pin PORENABLE/V_{PP} = 0), applying a high voltage to the PORENABLE/V_{PP} pin will also enable the POR circuit. This will cause a reset independent of the actual V_{DD} value.

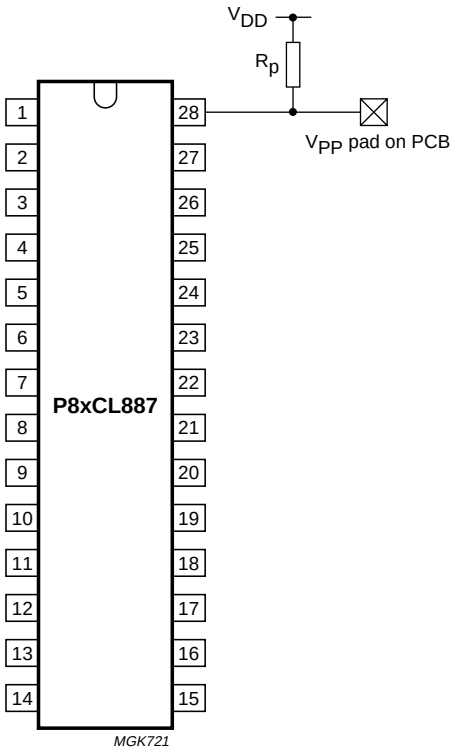


Fig.7 Example of PORENABLE/V_{PP} connection on a PCB.

6.7 Oscillator circuitry

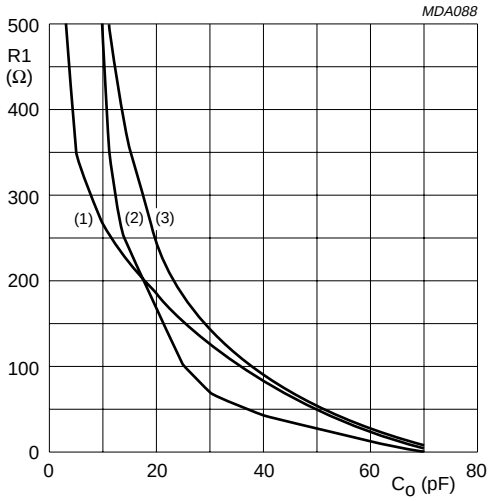
General information on the oscillator circuitry can be found in the *"TELX family"* data sheet.

6.7.1 Resonator requirements

For correct function of the oscillator, the values of R_1 and C_0 of the chosen resonator (quartz or PXE) must be below the line shown in Fig.8a. The value of the parallel resistor R_0 must be less than 47 kΩ. The wiring between chip and resonator should be kept as short as possible.

6.7.2 Recommended resonator types

- CSA 3.58MG (supplier Murata)
- FCR3.58M5 (supplier TDK).



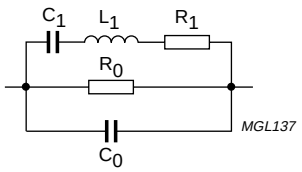
C_{1e} and C_{2e} are the external load capacitances; normally not needed due to integrated load capacitances of typically 10 pF.

(1) $C_{1e} = C_{2e} = 22$ pF.

(2) $C_{1e} = C_{2e} = 0$ pF.

(3) $C_{1e} = C_{2e} = 12$ pF.

a. Resonator curves.



b. Resonator equivalent circuit.

Fig.8 Resonator requirements for the ACO.

6.8 Emulation

The emulator for the P8xCL887 uses the P87CL880 microcontroller in emulation mode. The P87CL880 is a super-set of the P8xCL887, i.e. it contains all the functions of the P8xCL887 plus a number of other additional functions. It should be noted that some functional differences between the P87CL880 and the P8xCL887 exist; see Table 14.

Table 14 Differences between functions existing in P87CL880 and P8xCL887

FUNCTION	P87CL880	P8XCL887
Timer 2	see P87CL880 specification	see P8xCL887 specification
OTP Program Memory	32 kbytes AFPROM	12 kbytes EPROM or pre-programmed ROM
$\overline{EW}$ pin (Watchdog enable)	yes	no
Security concept	see P87CL880 specification	see P8xCL887 specification
In System Programming	no	yes
Reset value of SFRs	see P87CL880 specification	see P8xCL887 specification
POR	hardware programmable	fixed
Frequency	DC to 12.5 MHz	3.58 MHz
Read-Modify-Write bug	Yes	No

6.9 Read-Modify-Write bug

The first version of P87CL880 which is used in the emulator for the P8xCL887 contains a bug which affects all instructions of type Read-Modify-Write (RMW) to an I/O port. The instructions affected are: ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ, MOV Px.y, C, CLR Px.y and SET Px.y. Detailed explanations of the normal function of these instructions are explained in *"Data Handbook IC20"*.

The ports affected are port P0 and P3 on P87CL880.

Normally, a RMW instruction first reads the value which is present on the port latch (not the state of the port pins), modifies this value, and writes it back to the port latch.

Due to a critical timing between two internal signals in the present design, the RMW instructions do not work correctly.

Due to the bug, the RMW instructions on the port pins should be avoided. However, a software work around exist.

Instead of using the normal RMW instruction, each manipulation should be done on a copy-byte of the port latch (e.g. a bit addressable RAM byte for each port), and thereafter the new value of the copy-byte should be written to the port latch. It is important that any value to be written to a port must be copied in the copy-byte, see Example 1.

6.9.1 Example 1: Writing 'directly' to a port

Normally:

```
MOV P1,#53h          ;write value directly to port
```

Work-around:

```
MOV P1copy,#53h      ;write value to copy-byte
MOV P1,P1copy        ;write value of copy-byte to port
```

6.9.2 Example 2: Setting one bit of the port

Normally:

```
SET P1.0             ;set bit 0 of port P1
```

Work-around:

```
SET P1copy.0         ;set bit 0 of port P1copy, assuming register P1copy is chosen to
                     be in the bit addressable RAM area
MOV P1, P1copy       ;write value of copy-byte to port
```

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+4.0	V
V_I	input voltage on any pin with respect to ground (V_{SS})	–0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	–	800	mW
T_{stg}	storage temperature	–65	+150	°C

8 CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; V_{SS} = 0 V; f_{xtal} = 3.58 MHz; T_{amb} = –25 to +70 °C; (during In System Programming T_{amb} = 20 to 40 °C). All voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	operating		2.7	–	3.6	V
	RAM data retention in Power-down mode		1.0	–	3.6	V
	In System Programming		3.0	–	3.6	V
V_{PP}	OTP programming voltage		12.5	–	13.0	V
I_{DD}	operating supply current	V_{DD} = 3 V; note 1	–	–	2.0	mA
		V_{DD} = 3 V; T_{amb} = 25 °C; note 1; see Fig.9	–	1	–	mA
$I_{DD(id)}$	supply current Idle mode	V_{DD} = 3 V; note 2	–	–	0.55	mA
		V_{DD} = 3 V; T_{amb} = 25 °C; note 2; see Fig.10	–	0.26	–	mA
$I_{DD(pd)}$	supply current Power-down mode	V_{DD} = 3 V; T_{amb} = 25 °C; note 3; see Fig.11				
		POR and LVD enabled	–	2	5.0	µA
		POR and LVD disabled	–	100	–	nA
$I_{DD(block)}$	supply current per block:	V_{DD} = 3 V; T_{amb} = 25 °C; notes 4 and 5				
	DTMF	no load on TONE output	–	240	–	µA
	MSK modem		–	140	–	µA
	Watchdog		–	110	–	µA
	I^2C-bus		–	90	–	µA
	UART		–	90	–	µA
	Timer T2		–	90	–	µA
	Timer T0 or T1		–	5	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs (Ports, MIN, RST, MOUT0 to MOUT2 and PORENABLE)						
V_{IL}	LOW-level input voltage	notes 6 and 7	0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	note 6	$0.8V_{DD}$	–	V_{DD}	V
$\lvert I_{IL} \rvert$	LOW-level input current (ports in Mode 1)	V_{IN} = 0.4 V; note 8; see Fig.13	–	10	50	µA
$\lvert I_{IL(T)} \rvert$	LOW-level input current; HIGH-to-LOW transition (ports in Mode 1)	$V_{IN} = 0.5V_{DD}$; note 8; see Fig.13	–	200	1000	µA
$\lvert I_{LI} \rvert$	input leakage current (ports in Mode 0 or 2)	$V_{SS} \leq V_I \leq V_{DD}$	–	–	1	µA
Port outputs (Ports, RST and MOUT0 and MOUT2)						
I_{OL}	LOW-level output current; except P1.3, SDA, SCL and MOUT2	V_{OL} = 0.4 V	2	–	–	mA
I_{OL1}	LOW-level output current P1.3 (for LED)	V_{OL} = 0.4 V	6	–	–	mA
I_{OL2}	LOW-level output current; SDA, SCL and MOUT2	V_{OL} = 0.4 V; note 9	3	–	–	mA
I_{OH}	HIGH-level output current except P1.3; push-pull options only	$V_{OH} = V_{DD} - 0.4$ V	2	–	–	mA
I_{OH1}	HIGH-level output current P1.3 (for LED); push-pull options only	$V_{OH} = V_{DD} - 0.4$ V	6	–	–	mA
I_{OH2}	HIGH-level output current MOUT2	$V_{OH} = V_{DD} - 0.4$ V	3	–	–	mA
$I_{\overline{RST}}$	$\overline{RST}$ pull-up transistor current	V_{DD} = 3 V; $V_{OH} = V_{DD} - 0.4$ V	5	20	–	mA
		V_{DD} = 3 V; $V_{OH} = V_{SS}$	–	50	200	mA
Power-on-reset (POR); for the LVD (Low Voltage Detection) see note 10						
V_{PORH}	Power-on-reset trip level HIGH	option 5 in *"TELX family"* specification	2.13	2.37	2.61	V
V_{PORL}	Power-on-reset trip level LOW	option A in *"TELX family"* specification	1.98	2.27	2.56	V
TONE output (note 11 and Fig.12)						
$V_{HGF(rms)}$	HGF voltage (RMS)	V_{DD} = 3 V	158	181	205	mV
$V_{LGF(rms)}$	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	+0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	V_{DD} = 3 V; T_{amb} = 25 °C; notes 5 and 12	–	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
In System Programming for the OTP						
t_{prog}	program cycle time		90	100	110	µs
$t_{prog\ (security)}$	program cycle time security	note 13	180	200	220	µs
t_{ver}	verify cycle time		1	–	–	µs
$t_{Vpp(setup)}$	program voltage setup time		10	–	–	µs
$t_{Vpp(max)}$	maximum program voltage time	cumulative for the product lifetime	–	–	60	s
I_{Vpp}	program voltage current	In system programming	–	–	40	mA
ACO (Amplitude Controlled Oscillator)						
V_{XTAL1}	external clock signal amplitude peak-to-peak		500	–	V_{DD}	mV
$Z_{i(XTAL1)}$	input impedance on XTAL1		300	1000	–	kΩ
C_{1i}; C_{2i}	input capacitance on XTAL1 and XTAL2	notes 5 and 14	–	10	–	pF

Notes

1. The operating supply current is measured with all output pins disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; $\overline{RST} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; fetch of NOP instructions; all derivative blocks disabled.
2. The Idle mode supply current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; all derivative blocks disabled.
3. The Power-down current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 and XTAL2 not connected.
4. The typical currents are only for the specific block. To calculate the typical power consumption of the microcontroller, the current consumption of the CPU must be added. Example: the typical current consumption of the microcontroller in operating mode with CPU, Watchdog Timer and UART active can be calculated as (1 + 0.11 + 0.09) mA = 1.2 mA.
5. Verified on sampling basis.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I^2C-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1.
7. For the PORENABLE pin, $V_{IL(max)}$ is $0.1V_{DD}$.
8. Not valid for pins SDA, SCL, $\overline{RST}$, MIN and PORENABLE.
9. The maximum allowed load capacitance C_L is in this case limited to approximately 200 pF.
10. The LVD is tested according to the specification in the data sheet *"TELX family; Chapter: Low Voltage Detection"*.
11. Values are specified for DTMF frequencies only (CEPT CS203).
12. Related to the Low Group Frequency (LGF) component (CEPT CS203).
13. Can also be done by two 100 µs pulses.
14. C_{1i} and C_{2i} are the total internal capacitances (including gate capacitance and leadframe capacitance).

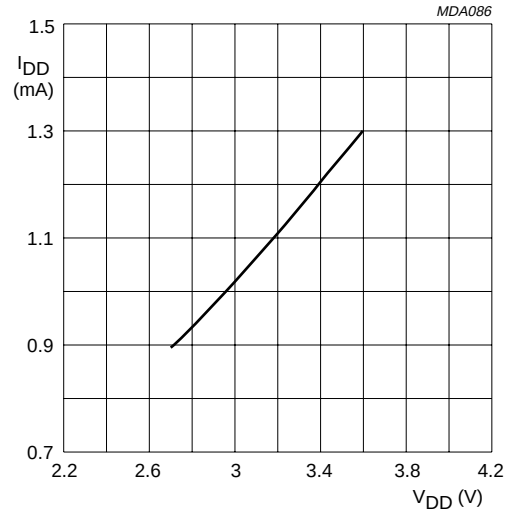


Fig.9 Typical operating current as a function of V_{DD}; T_{amb} = 25 °C.

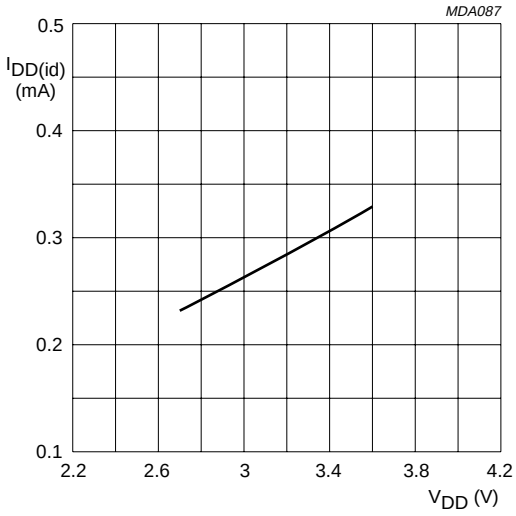
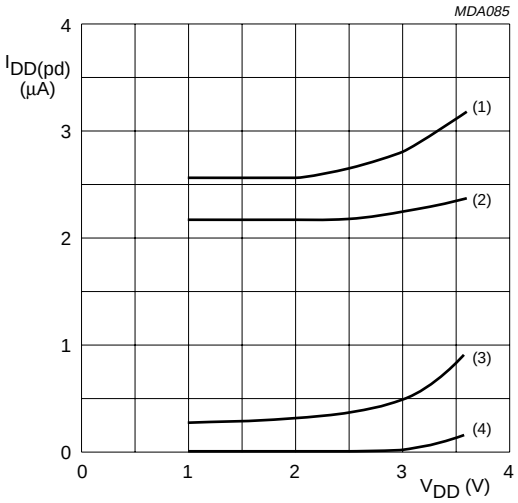
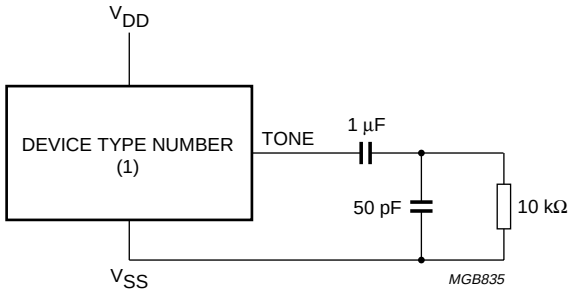


Fig.10 Typical Idle current as a function of V_{DD}; T_{amb} = 25 °C.



(1) POR and LVD enabled (T_{amb} = 70 °C).
(2) POR and LVD enabled (T_{amb} = 25 °C).
(3) POR and LVD disabled (T_{amb} = 70 °C).
(4) POR and LVD disabled (T_{amb} = 25 °C).

Fig.11 Typical Power-down current as a function of V_{DD}.



(1) P83CL887/P87CL887

Fig.12 TONE output test circuit.

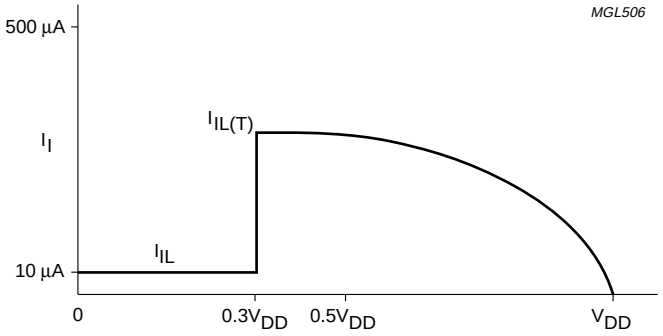
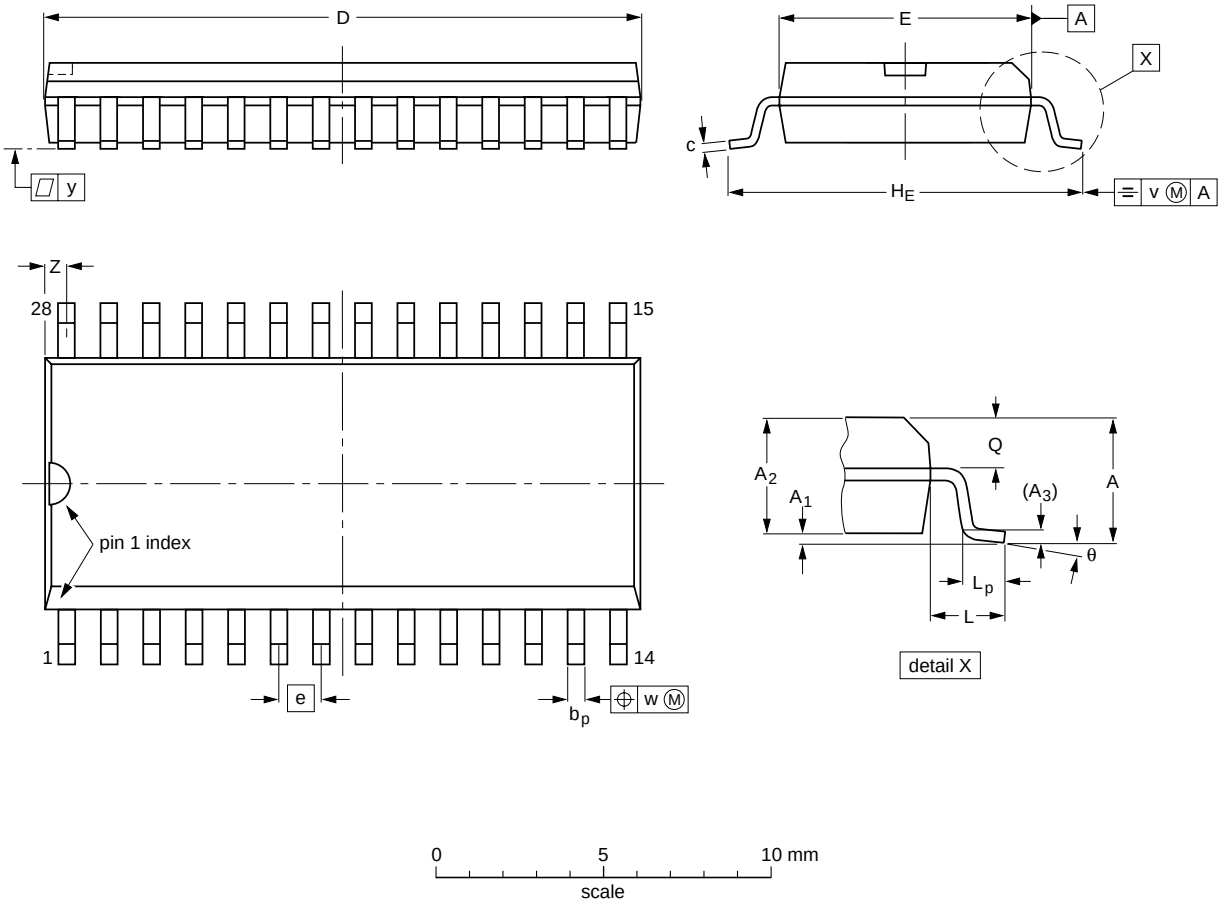


Fig.13 Input current.

9 PACKAGE OUTLINE

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

10 SOLDERING

10.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

10.2 Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

10.3 Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

10.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

11 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

12 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

13 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands 457047/00/01/pp32 Date of release: 1997 Oct 30 Document order number: 9397 750 02648

Let's make things better.

Philips Semiconductors

PHILIPS